

REMARKS

Favorable reconsideration of this application, as amended, is respectfully requested.

Without concession as to the propriety of the outstanding rejection, the independent claims have been amended to more particularly claim certain aspects of the invention.

Independent Claim 1 has been amended to recite, *inter alia*, that the memory controller controls access to a first address of a first non-volatile memory and the first address of a second non-volatile memory, when both of the first address of the first non-volatile memory and the first address of the second non-volatile memory are valid, and wherein the memory controller controls access to a second address of the first non-volatile memory and a third address of the second non-volatile memory, when the second address of the second non-volatile memory is invalid.

Independent Claim 2 has been amended to recite, *inter alia*, that the memory controller controls access to a first address of the first non-volatile memory and the first address of the second non-volatile memory, when both of the first address of the first non-volatile memory and the second address of the second non-volatile memory do not include an error memory cell, and wherein the memory controller controls access to a second address of the first non-volatile memory

and a third address of the second non-volatile memory, when the third address of the second non-volatile memory includes an error memory cell.

Independent Claim 8 has been amended to recite, *inter alia*, that the control circuit is capable of accessing a first address of a first non-volatile memory and the first address of a second non-volatile memory in parallel, when both of the first address of the first non-volatile memory and the first address of the second non-volatile memory are valid, and wherein the control circuit is capable of accessing a second address of the first non-volatile memory and a third address of the second non-volatile memory in parallel, when the second address of the second non-volatile memory is invalid.

Independent Claim 9 has been amended to recite, *inter alia*, that the memory controller is capable of accessing a first address of the first non-volatile memory and the first address of the second non-volatile memory in parallel, when both of the first address of the first non-volatile memory and the first address of the second non-volatile memory do not include an error memory cell, and wherein the memory controller is capable of accessing a second address of the first non-volatile memory and a third address of the second non-volatile memory in parallel, when the third address of the second non-volatile memory includes an error memory cell.

Independent Claim 13 has been amended to recite, *inter alia*, that the wherein said control circuit is adapted to access a first address of a first non-volatile memory and said first address of a second non-volatile memory in parallel, when both of said first address of said first non-volatile memory and said first address of said second non-volatile memory do not include an error memory cell, and wherein said control circuit is adapted to access a second address of said first non-volatile memory and a third address of said second non-volatile memory in parallel, when a second address of said third non-volatile memory includes an error memory cell.

Estakhri suffers from the same drawbacks as discussed in Applicants' background of the invention as at least discussed on page 2. Specifically, in Estakhri, if either a corresponding pair of non-volatile memory locations 732, 733 is determined to be defective, then the whole memory block 727 is declared to be defective... and the defective block can no longer be used. (emphasis added)

In that Estakhri at least does not teach or suggest the above enumerated features, independent Claims 1, 2, 8, 9 and 13 are patentably distinguishable therefrom.

A Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16

and 1.17 that may be required by this paper and to credit any overpayment to that Account.

If any extension of time is required in connection with the filing of this paper and has not been requested separately, then such extension is hereby requested.

Respectfully submitted,

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